REMARKS

This amendment is being filed in response to the Office Action having a mailing date of July 24, 2008. Claims 13 and 17 are amended as shown. Claim 25 is canceled herein without prejudice. With this amendment, claims 1-24 are pending in the application.

I. Rejections under 35 U.S.C. 112

The present Office Action rejected claim 25 under 35 U.S.C. § 112. While it is believed that such rejection(s) of claim 25 do not have merit, claim 25 is nevertheless canceled herein without prejudice so as to facilitate prosecution and to reduce the number of issues under dispute.

The present Office Action further rejected previously presented claims 13-16 and 17-20 under 35 U.S.C. § 112, first paragraph, for allegedly failing to comply with the written description requirement. Specifically, page 3 (section 6) of the present Office Action alleged that "signal generating means for generating and transmitting on said single line an identity signal, in addition to at least one signal that transmits said data" was not described in the original disclosure. This written rejection of claims 13-16 and 17-20 is respectfully traversed herein.

For example, page 23, lines 12-24 of the present application describes generation and transmission of the "identity signal" in addition to the "n-bit datum to be transmitted." Furthermore, Figures 5 and 9 (and the accompanying description in the present application) disclose the "Data OUT" signal (the signal that transmits said data) that is generated and transmitted by the data source 10, the transmitter 11, and the FIFO 12 (for the embodiment of Figure 5). In Figures 5 and 9 (and the accompanying description in the present application), the identity signal is depicted as the "Sync" signal that is generated and transmitted by at least one finite state machine (FSM) 13, with the Sync signal being the signal through which the sorting pattern used for transmission is identified.

In view of the above-identified and other disclosure provided by the present application, it is therefore respectfully submitted that claims 13-16 and 17-20 meet written description requirements. Accordingly, it is kindly requested that the rejections under 35 U.S.C. § 112, first paragraph be withdrawn.

Claims 13 and 17 are amended as shown to more precisely recite the generation and transmission of the identity signal and the at least one signal that transmits said data.

II. Discussion of the claims and cited references

The present Office Action continued to reject claims 1-24 under 35 U.S.C. § 103(a) as being unpatentable over Curran (U.S. Patent No. 5,572,736) in view of Szepesi (U.S. Patent No. 5,680,300). Claim 25 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Curran and Szepesi in view of Rui (U.S. Patent Application Publication No. 2002/0196327).

With the cancellation of claim 25 without prejudice herein, the rejection of claim 25 is rendered moot. For the reasons set forth below, the rejections of claims 1-24 are respectfully traversed. It is therefore kindly requested that these rejections be reconsidered and withdrawn.

A. Independent claim 1

Independent claim 1 as presented herewith recites, *inter alia*, "transmitting on at least one line of the bus the datum in said transmission format, and transmitting on one additional line of the bus a synchronization signal having the selected sorting pattern." These limitations make it clear that there are two pieces of information being transmitted on respective two lines of the bus: (a) the datum, and (b) the synchronization signal having the selected sorting pattern. Since these two pieces of information are being sent on two respective separate/different bus lines (*i.e.*, the "at least one line" and the "one additional line"), it is therefore inherent/explicit that the datum and synchronization signal having the sorting pattern are not one and the same signal(s) in claim 1.

It is respectfully submitted that these various limitations recited in claim 1 are not met by the cited references, whether singly or in combination.

For example, page 5 (section 12) of the present Office Action relies upon Curran's column 2, lines 60-65 as teaching "transmitting on the bus the selected sorting pattern

(switching code identifying the mapping code…)." Curran explains the following in his column 2, lines 60-65 and in column 4, lines 43-49 (emphasis ours):

> "In accordance with another aspect of the invention, a switching code identifying the mapping code used in the mapping of the data word into the n-bit code word selected for transmission is incorporated in the transmitted code word and is used in the receiving circuit to map the received code word into the original data word, as that data word existed prior to transmission … a plurality of mapping codes are generated, each identified by the state of the switch bits. Each mapping code is applied to the new data word and in each case, selected bits of the data word are complemented and the switch bits are appended to the resultant word to form a code word."

From the above-quoted passages of Curran, it is therefore abundantly clear that Curran's switching code "is incorporated in" the transmitted code word. Stated in another way, Curran transmits his switching code and data word together as one signal on the same/single line, since he "incorporates" or "appends" this information together. Indeed, Curran further teaches that his data word and switching code are transmitted in the same signal as a "code word," in his column 3, lines 5-8 that teaches "a code word is generated by applying a mapping code to the data word to be transmitted and adding a switching code," and in column 3, lines 13-17 that teaches "a code word transmitted on the data transmission bus to generate a code word representative of an input data word and comprising a switching code defining selected bits of the data word which have been complemented" (emphasis ours).

Thus from the above-quoted passages of Curran, by "incorporating" or "appending" his switching code ("switch bits") into the transmitted code word, Curran inherently/explicitly cannot meet the limitations of claim 1 that require at least one line of the bus to transmit the datum and an additional line of the bus to transmit the selected sorting pattern (via the synchronization signal). Curran's technique of incorporating his switching code into the

transmitted code word means that these two things (switching code and data/code word) are transmitted together on the same line in Curran, rather than on separate/multiple lines as reflected in claim 1.

Page 6 (section 12) of the present Office Action indeed acknowledged that Curran does not teach "transmitting on one additional line of the bus the selected sorting pattern." Nevertheless, page 6 (section 12) of the present Office Action alleged the following (emphasis ours):

> "It would have been obvious; to a person having ordinary skill in the art, at the time that the invention was made, that the two above limitations are obvious variants of one another. In the first limitation, the selected sorting pattern is transmitted and received on the bus. The variant is the selected sorting pattern is transmitted on one additional line of the bus. A person having ordinary skill in the art would recognize that the functionality of the two structures is the same. The second structure has an additional line; however, the information that was originally carried on one bus is now carried on two communication lines."

The present Office Action's allegations that the two techniques are "obvious variants" of one another and that "the functionality of the two structures is the same" are respectfully traversed herein.

It is well settled that if a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Moreover, if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

In the present situation, the Office Action has alleged above that an obvious variant of Curran is to transmit Curran's switching code (construed by the present Office Action as the claimed "selected sorting pattern") on one additional line of the bus. It is respectfully submitted that such a proposed modification of Curran would render his invention "unsatisfactory for its intended purpose" and/or "would change the principle of operation" of his invention, and therefore such a proposed modification would not render claim 1 *prima facie* obvious.

For example, Curran needs to incorporate/append his switching code into his transmitted code word in a manner that the data word and the switching code are transmitted together, so that the number of bits in the code word is n + s, where n is the number of bits in the data word and n is the number of switch bits. These values of n + s, n, and s are then used to compute a Hamming distance, lowest Hamming distance, the number of switching drivers, etc. Curran teaches the following in his column 4, line 46 to column 5, line 21 (emphasis ours):

> "Each mapping code is applied to the new data word and in each case, selected bits of the data word are complemented and the switch bits are appended to the resultant word to form a code word. The number of bits in the code word is equal to n+s, where n is the number of bits in the data word and s is the number of switch bits. Each of the code words is compared with a previously transmitted code word and the Hamming distance between each of the generated code words and the previously transmitted code word are computed. The code word with the lowest Hamming distance is selected and transmitted in the next bus cycle. A decoder at the receiving end decodes the switch bits and applies a reverse mapping as identified by the switch bits to recover the original data word.
>
> An upper bound on the improvement is obtained by a maximally distant mapping code. Consider the volume of a sphere in p-dimensional space to be the number of p-dimensional points residing on or within this sphere. The entire volume of a p-dimensional space is 2^p, since that is the

total number of points in this space. Let the 2^S mappings of an (n, n+s) code define the origins of 2^S zero-radius spheres in the n+s dimensional space. The initial volume of each of these spheres is 1 since they each contain one point. Simultaneously grow the radius of these spheres until all points in the n+s dimensional space at r contained within at least one sphere. The final radius of the spheres, r is the maximum number of switching drivers since every code word in the n+s dimensional space is within a distance r of one of the mappings. The distance r must satisfy the following equation:

$$2^S \{ 1 + \sum_{k=1}^{r} (n+s)!/k!(n+s-k)! \} \geq 2^{(n+s)}$$

wherein (n + s)!/k!(n + s –k)!

defines the number of points which are located at exactly a distance k from a sphere origin. The equation states that the volumes of the 2^S spheres must be equal to or greater than the volume of the entire code space. It can be shown that for the various values of n, s, r the maximum improvement in the delta-I noise is greater than 50 percent for all cases and nearly 70 percent in certain cases."

From the above-quoted passage of Curran, it is abundantly clear that the number of bits (n + s) of the code word having the switching code incorporated therein, the value n, and the value s are crucial in determining his number of switching drivers r, the lowest Hamming distance, etc. These values, in particular the number of bits (n + s) in the code word, can only be obtained by appending the switching code to the data word, and the Hamming distances are computed between such generated and previously generated code words that have these number of bits (n + s).

It is respectfully submitted that modification of Curran as suggested by the present Office Action, such that the switching code is sent on a different bus line than the data word, would not be able to provide the total number of bits (n + s) of the code word as taught above, and would further not allow the Hamming distance computation as taught above in which the Hamming distance between each of the generated code words and the previously transmitted code word are computed. For example, if the data word of Curran does not have the switching code appended thereto, the quantity (n + s) would not exist at all, and therefore the equation above cannot be computed and the Hamming distances between code words having numbers of bits (n + s) cannot be determined since the resulting code words for Hamming computation would just have the number of bits n.

Accordingly therefore, a modification as proposed by the present Office Action would render Curran's invention "unsatisfactory for its intended purpose" and/or "would change the principle of operation" of his invention, and therefore such a proposed modification would not render claim 1 *prima facie* obvious.

Furthermore, Curran is substantially a reworking of a conventional technique known as "bus-inverter", which is a redundant encoding technique that associates the n-bit encoded information with a redundancy which is made up of s-bit switching bits and which specifies which lines are to be complemented at the reception end to recover the original information. Curran discloses a switching code that identifies the bus lines that are to be inverted, and is a string as long as the number of bus lines: when a bit in the i-th position is "1", the corresponding bus line is to be complemented at the reception end to recover the information transmitted. A 16-line bus has thus a switching code of the type "0001001011010011". In comparison, one embodiment provided by the present applicant involves, instead, the swapping pattern being a bit sequence that indicates the bus lines that are to be multiplexed, and is M.log2(M) long, where M is the bus switch cluster depth. If N=4, then the swapping pattern is 8 bit long. For example, a valid swapping pattern (namely a pattern that allows the transmitted information to be validly recovered at the reception end) is 0-2-3-1 (00101101 in binary). Not all the swapping patterns may be valid. For example, 0-1-0-3 (00010011 in binary) may not allow the transmitted information to be validly recovered at the reception end.

Claim 1 as presented herewith is still further allowable over the cited references in that there are two synchronizations provided in claim 1. First, there a first synchronization using the above-discussed synchronization signal that provides the selected sorting pattern. Second, there is a second synchronization involving synchronization of sorting patterns using a same clock signal: "a succession of said sorting patterns generated at a transmission end and a succession of sorting patterns generated at a reception end are synchronized with each using a same clock signal supplied to said transmission and reception ends."

The present Office Action admitted on page 5 (section 6) that "Curran may not explicitly teach push-pull bus driver used for synchronization." To supply these missing synchronization teachings of Curran, the present Office Action alleged that the push-pull driver disclosed in Szepesi's column 6, lines 18-34 provides synchronization. It is respectfully submitted that Szepesi does not cure the deficiencies of Curran.

More particularly, assuming *hypothetically* and *arguendo* that Szepesi's push-pull driver does provide synchronization, Szepesi nevertheless does not disclose, teach, or suggest that a synchronization signal provided by his push-pull driver would be providing informational content (specifically, "a synchronization signal having the selected sorting pattern" as recited in claim 1). Rather, Szepesi's synchronization signal is used merely for clocking. Column 6, lines 18-34 of Szepesi relied upon by the present Office Action is reproduced below (emphasis ours):

> "The synchronization block 22, under control of the phase 2 clock output θ_2, cuts off the drive to sw4 during the first phase θ_1 of the clock; during phase 2 (θ_2 low), the synchronization block 22 enables sw4 to be driven. That is, during the clock's second phase θ_2 an analog switch 40 provides an analog signal path, i.e., one which accommodates a continuously variable signal, from the output of the amplifier 36 to the push-pull stage 38. During this phase, the gate voltages to n-channel FETs 42 and 44 are low, consequently FETs 42 and 44 are 'OFF' and the output of the amplifier 36 is conducted through the analog switch 40 and drives the push-pull stage 38 which, in turn, modulates the gate voltage of sw4.

> During phase 1 θ_2 is high, therefore analog switch 40 is non-conducting and FETs 42 and 44 are 'ON', shutting off drive current to the push pull stage 38 and turning sw4 'OFF'."

From the above-quoted passage of Szepesi relied upon by the Office Action, it is evident that Szepesi does not provide a synchronization signal that has informational content (namely, a synchronization signal having the selected sorting pattern)— Szepesi only provides clocking, as taught in his passage quoted above. Since neither Curran nor Szepesi meet the limitations of claim 1 that require "a synchronization signal having the selected sorting pattern", claim 1 is allowable.

For all of the above reasons, it is thus respectfully submitted that claim 1 is allowable.

B. Independent claims 8 and 12

Independent claims 8 and 12 generally recite features similar to claim 1, using varying language. Specifically, claim 8 as presented herewith recites, *inter alia*, the features of the synchronization signal having the optimal sorting pattern, transmitting the datum on at least one line, and transmitting the optimal sorting pattern (via the synchronization signal) on one additional line. Furthermore, claim 8 recites synchronization of sorting patterns using a same clock signal, thereby also providing claim 8 with two synchronizations (the synchronization signal having the optimal sorting pattern and the synchronization of the sorting patterns using the same clock signal).

Claim 12 as presented herewith also recites, *inter alia*, the features of the synchronization signal having the selected sorting pattern, transmitting the datum on at least one line, and transmitting the selected sorting pattern (via the synchronization signal) on one additional line. Furthermore, claim 12 recites synchronization of sorting patterns using a same clock signal, thereby also providing claim 12 with two synchronizations (the synchronization signal having the optimal sorting pattern and the synchronization of the sorting patterns using the same clock signal).

As previously explained above, Curran and Szepesi (whether singly or in combination) do not meet these limitations. For example, Curran does not send his data word and switching code on a respective at least one line and at least one additional line. Further, two signals to provide synchronization are recited in these claims, whereas the cited references do not provide the recited two signals to synchronize and further Szepesi provides a signal only for clocking, and such a signal does not have the sorting pattern as claimed.

Hence, claims 8 and 12 are allowable.

C. Independent claims 13, 17, and 22

Independent claims 13 and 17 presented herewith recite, *inter alia* and using varying language, further generating and transmitting in addition to said identity signal at least one signal that transmits said data. Hence, it is clear in claims 13 and 17 that the identity signal is separately/additionally transmitted from the data signal. As previously explained above, Curran does not meet these limitations, since he appends/incorporates his switching code (switch bits) into his transmitted code word, thereby transmitting them together in one signal (rather than as two signals as required in claims 13 and 17).

Independent claim 22 as presented herewith recites, *inter alia*, that the datum is transmitted on at least one line and the synchronization signal is transmitted on one additional line. Again, Curran does not meet these limitations since he appends/incorporates his switching code into his code word, thereby transmitting them together on the same line.

Claim 22 is also further allowable since two synchronizations are recited (synchronization signal and synchronization of the sorting patterns using a same clock signal). This dual synchronization is not provided by either of the cited references, which at most provide only a singular synchronization.

Accordingly, claims 13, 17, and 22 are allowable.

III. Conclusion

If the attorney of record (Dennis M. de Guzman) has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested

to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact Mr. de Guzman at (206) 622-4900.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are believed to be allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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